REMARKS

I. Introduction

Applicants note with appreciation the indication of allowable subject matter recited in claims 14 and 15.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 11 And 12 Under 35 U.S.C. § 103

Claims 11 and 12 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Jarwala et al. (USP No. 5,673,276) in view of Komoike (USP No. 6,094,736) and Yamamura (USP No. 5,341,096). Applicants respectfully traverse these rejections for at least the following reasons.

Claim 11 recites, in part, a semiconductor device comprising...an internal scan chain for an internal scan test provided in each of said chip IPs, a logic circuit which is a test object (DUT) in said chip IPs to be tested by said internal scan test; and wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an internal scan test simultaneously with each other for testing said test object (DUT), using test data for an internal scan test which is input from outside.

One feature of the present invention is that is uses test data for an internal scan test which is input from outside. As a result, the semiconductor of the present invention can readily detect failures with a higher detection rate than that of Yamamura.

It is alleged that Yamamura discloses that it is possible to operate the boundary scan test circuit and the internal scan chain simultaneously during an internal scan test, and a test object (DUT) in each of the chip IPs.

However, Yamamura fails to disclose a semiconductor device that uses test data for an internal scan test which is input from outside. Yamamura discloses a circuit having a built-in self test (BIST) mechanism that when the boundary scan test circuit and the internal scan chain are simultaneously operated, a periodic pattern generated in an *internal* circuit and a random pattern data are used as test data (see, col. 6, lines 6-26 and col. 8, lines 36-57 of Yamamura). Thus, the test data is not input from the outside, but rather from the inside.

Furthermore, it is well known in the art, such as Yamamura, that LSIs have been configured so that a boundary scan test and a built-in self test can be operated simultaneously. However, the prior art also shows that LSIs cannot operate a boundary scan test and *an internal scan test* simultaneously during an internal scan test using data input from the outside. Thus, the object of Yamamura is different to that of the present invention. As such, it is clear that Yamamura fails to disclose the above cited limitation of claim 11.

Komoika and Jarwala do not cure this deficiency of Yamamura, and are not relied upon as doing so.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA1974). As Jarwala, Komoike and Yamamura, at a minimum, each fail to teach or suggest a semiconductor device with the limitations recited above, it is submitted that the combination of Jarwala, Komoike and Yamamura does not render claim 11 obvious. Accordingly, it is respectfully requested that the § 103 rejection of claim 11, and any pending claims dependent thereon be withdrawn.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 11 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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